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Atsushi

TITLE: Dry etching method for gate electrode formation in MOS transistor - involves changing side wall protective film thickness, to perform dry etching

PRIORITY-DATA: 1998JP-0017435 (January 29, 1998)

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PATENT-FAMILY:

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INT-CL (IPC): H01 L 21/3065; H01 L 29/78

ABSTRACTED-PUB-NO: JP 11220123A
BASIC-ABSTRACT:

NOVELTY - Film thickness of side wall protective film is changed and dry etching is performed to form a gate electrode of predetermined pattern.

USE - For gate electrode formation in MOS transistor.

ADVANTAGE - Prevents generation of side etching resulting from difference of etching rate caused during gate electrode formation, since side wall protective film thickness is modified.

DESCRIPTION OF DRAWING - The figure is a sectional view of dry etching process for gate electrode formation.

PATENT ABSTRACTS OF JAPAN

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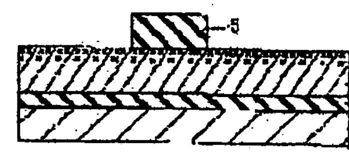
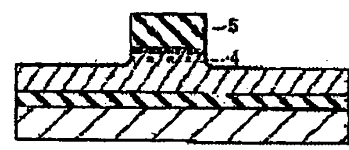
(21)Application number : 10-017435
(22)Date of filing : 29.01.1998

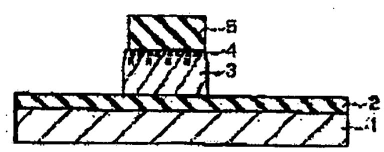
(71)Applicant : SONY CORP
(72)Inventor : KAWASHIMA ATSUSHI

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress the occurrence of side etching caused by the difference in etching rate, and to suppress the increase in resistance following the effect of fine wire by a method wherein dry etching is performed by changing the thickness of a side wall protective film for formation of an element formation layer using the side wall protective film.
SOLUTION: First, the natural oxidation film on the surface of a polysilicon layer is removed by etching. Subsequently, the impurity-doped part on the surface of the polysilicon film 3 is dry-etched by using both dry etching gas and side wall protection film forming gas. Then, the non-doped part of the lower layer section of the polysilicon film 3 is dryetched using both dry-etching gas and the side wall protection film forming gas. When the polysilicon film 3 is dry-etched by using the side wall protecting film, dry etching treatment is performed while the thickness of the side wall protecting film is being changed in accordance with the concentration of impurities contained in the layer of the polysilicon film 3.







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(71)出願人　000002185
ソニー株式会社
東京都品川区北品川6丁目7番35号

(72)発明者　川島　淳志
東京都品川区北品川6丁目7番35号　ソニー株式会社内

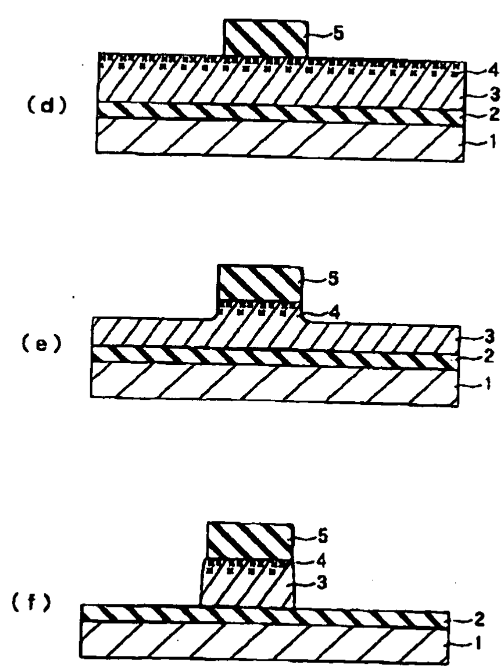
(74)代理人　弁理士　佐藤　隆久

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】

【課題】側壁保護膜を用いながらドライエッチングにより素子形成層を所定のパターンに形成する際に生じるエッチングレートの相違に起因するサイドエッチングの発生を防止し、サリサイド工程により形成されるチタニウムシリサイド等の金属シリサイドの形成面積が小さくなって、いわゆる細線効果に伴う抵抗上昇を抑制して、信頼性の高い半導体装置を製造する製造方法を提供する。

【解決手段】素子形成層を側壁保護膜を用いて所定のパターンに形成するためのドライエッチング工程を有する半導体装置の製造方法において、前記ドライエッチング工程は、側壁保護膜の膜厚が厚い状態でドライエッチングを行う工程と、側壁保護膜の膜厚が薄い状態でドライエッチングを行う工程とからなる半導体装置の製造方法。



【特許請求の範囲】

【請求項1】素子形成層を側壁保護膜を用いて所定のパターンに形成するためのドライエッチング工程を有する半導体装置の製造方法において、
前記ドライエッチング工程は、
側壁保護膜の膜厚を変化させてドライエッチングを行う工程である、
半導体装置の製造方法。

【請求項2】前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、
側壁保護膜の膜厚が厚い状態でドライエッチングを行う工程と、
側壁保護膜の膜厚が薄い状態でドライエッチングを行う工程とからなる、
請求項1記載の半導体装置の製造方法。

【請求項3】前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、
エッチングガスに対するエッチングレートに応じて側壁保護膜の膜厚を変化させながらドライエッチングを行う工程である、
請求項1記載の半導体装置の製造方法。

【請求項4】前記側壁保護膜の膜厚が厚い状態でドライエッチングを行う工程は、
不純物がドーピングされたポリシリコン膜をエッチングする工程である、
請求項1記載の半導体装置の製造法。

【請求項5】前記側壁保護膜を形成しながら所定のパターンを形成するためのドライエッチング工程は、
ゲート電極を形成する工程である、
請求項1記載の半導体装置の製造方法。

【請求項6】前記不純物は周期律表の5B族元素である、
請求項4記載の半導体装置の製造法。

【請求項7】前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、
前記ポリシリコン膜の不純物がドーピングされた部分をエッチングする際における前記側壁保護膜の膜厚を、前記ポリシリコン膜の不純物がドーピングされていないポリシリコン膜をエッチングする際における前記側壁保護膜の膜厚よりも厚くしながらエッチングする工程である、
請求項1記載の半導体装置の製造法。

【請求項8】前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、
前記ポリシリコン膜の不純物がドーピングされた部分をエッチングする際における前記側壁保護膜形成用のガス量を、前記ポリシリコン膜の不純物がドーピングされていない部分をエッチングする際における前記側壁保護膜形成用ガス量よりも多く用いてエッチングする工程である、
請求項1記載の半導体装置の製造法。

【請求項9】前記側壁保護膜形成用のガスは、臭化水素である、
請求項8記載の半導体装置の製造法。

【請求項10】前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、
反応性イオンエッチング（Reactive Ion Etching）である、
請求項1記載の半導体装置の製造法。

【請求項11】前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、
エッチング用ガスとして、塩素、酸素および臭化水素を含有するガスを用いる工程である、
請求項1記載の半導体装置の製造法。

【請求項12】半導体基板上に絶縁膜を形成する工程と、
該絶縁膜上にポリシリコンからなる層を形成する工程と、
該ポリシリコンからなる層に不純物をドーピングする工程と、
前記ポリシリコンからなる層の不純物がドーピングされた部分を、側壁保護膜の膜厚が厚い状態でドライエッチングを行う工程と、
前記ポリシリコンからなる層の不純物がドーピングされていない部分を側壁保護膜が薄い状態でドライエッチングを行う工程とを有する、
半導体装置の製造方法。

【請求項13】前記不純物は、周期律表の5B族元素である、
請求項12記載の半導体装置の製造法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置の製造方法、特にMOS（Metal Oxide Semiconductor）トランジスターのゲート電極形成工程において使用されるドライエッチング方法に関する。

【0002】

【従来の技術】近年、半導体装置の分野ではますます集積化が進行して、例えば、超ＬＳＩについてその構造の微細化が進み、微細加工技術への要求は益々厳しいものとなってきている。例えば、ポリシリコンをはじめとするシリコン系材料を用いたゲート加工に関しても、異方性と高選択比を両立するプロセスの開発が望まれている。

【0003】ところで、酸化膜以外の材料をプラズマエッチングにより、例えば、素子形成層を所定のパターンで形成する場合において、その異方性形状の確保については、プラズマエッチング時に生成した反応生成物がプラズマ中で再解離することにより、層の側壁に保護膜（以下、「側壁保護膜」という。）を形成しながら、エ

ッチングを行う手法が採られている。
【0004】また、最近の半導体装置の構造の微細化に伴い、素子形成層等の寸法格差の絶対値とそのばらつきが問題となってきた。その為の対策として、例えば、高速排気を行いつつエッチングすることにより、エッチング処理中におけるエッチングガスの滞留時間を短くする方法が採用されてきている。
【0005】しかし、上記の方法では、エッチング処理中におけるエッチングガスの滞留時間が短くなる結果、エッチング処理中に反応生成物がプラズマ中で再解離するのが抑制され、堆積物が減少し、側壁保護膜が薄膜化する。側壁保護膜が薄膜化すると、サイドエッチングが進みすぎたり、ノッチングと呼ばれる現象が生じ、素子形成層等の寸法格差の絶対値とそのばらつきの問題は解決されない。
【0006】このための対策として、基板印加バイアスを上昇させる方法もあるが、今度は下地のゲート酸化膜とのエッチングに対する選択比の低下や、プラズマダメージ発生による酸化膜劣化のおそれがある。
【0007】一方、半導体装置において、ポリシリコン膜を電極材料あるいはコンタクト材料として用いる場合、通常、化学的気相成長法（ＣＶＤ法）又はスパッタリング法等により、ポリシリコン膜を成長させたのち、イオン注入法又は拡散法等で、リン、ホウ素等の不純物をポリシリコン中にドーピングし、熱処理を行っている。このように不純物を含有したポリシリコン膜をゲート酸化膜上のゲート電極として用いた場合、ポリシリコン膜成長後に加えられる熱処理によって、不純物がゲート酸化膜に拡散してその膜質に劣化をもたらす。
【0008】それを避けるため、熱処理を行わずにゲート電極の加工、すなわち、不純物を含有したポリシリコン膜のドライエッチングを行う手法が知られている。
【0009】
【発明が解決しようとする課題】しかし、上記熱処理を行わない手法では、ドーピングした不純物はポリシリコン表層部に偏って存在することになり、リン、砒素等の周期律表５Ｂ族元素であるｎ型ドーパントをドーピングした部分は、ドーピングしないポリシリコンと比較してエッチングレート（エッチングされ易さ）が大きいため、ｎ型不純物がドーピングされたポリシリコン膜の表層部に局所的にサイドエッチングが入る問題がある（図７（ａ），（ｂ）参照）。このようなサイドエッチングは、前述のような高速排気プロセスによる側壁保護膜の薄さに加え、ｎ型ドープドポリシリコンにおいて生じるエッチングレートの増速に起因している。
【0010】サイドエッチングが発生すると、段差被覆性に優れたサイドウォールスペーサ形成用の窒化シリコン膜がこのサイドエッチング部に入り込み、サイドエッチング部においては、ゲート電極上面が覆われてしまうことになる（図７（ｃ）及び図８（ｄ），（ｅ）参照）。
【0011】従って、後のサリサイド工程により形成されるチタニウムシリサイド等の金属シリサイドの形成面積が小さくなり、いわゆる細線効果に伴う抵抗上昇をもたらし、半導体装置の信頼性の低下につながるおそれがある。
【0012】本発明は、側壁保護膜を用いながらドライエッチングにより素子形成層を所定のパターンに形成する際に生じるエッチングレートの相違に起因するサイドエッチングの発生を防止し、サリサイド工程により形成されるチタニウムシリサイド等の金属シリサイドの形成面積が小さくなって、いわゆる細線効果に伴う抵抗上昇を抑制して、信頼性の高い半導体装置を製造する製造方法を提供することを目的とする。
【0013】
【課題を解決するための手段】本発明は、かかる目的を達成すべく、素子形成層を側壁保護膜を用いて所定のパターンに形成するためのドライエッチング工程を有する半導体装置の製造方法であって、前記ドライエッチング工程は、側壁保護膜の膜厚を変化させてドライエッチングを行う工程である半導体装置の製造方法を提供する。
【0014】本発明の半導体装置の製造方法において、前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、好ましくは、側壁保護膜の膜厚が厚い状態でドライエッチングを行う工程と、側壁保護膜の膜厚が薄い状態でドライエッチングを行う工程とからなる半導体装置の製造方法である。
【0015】本発明の半導体装置の製造方法において、前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、好ましくは、エッチングガスに対するエッチングレートに応じて側壁保護膜の膜厚を変化させながらドライエッチングを行う工程である半導体装置の製造方法である。
【0016】本発明の半導体装置の製造方法においては、前記側壁保護膜の膜厚が厚い状態でドライエッチングを行う工程は、好ましくは、不純物がドーピングされたポリシリコン膜をエッチングする工程であり、前記側壁保護膜を形成しながら所定のパターンを形成するためのドライエッチング工程は、ゲート電極を形成する工程であり、前記不純物は周期律表の５Ｂ族元素が好ましい。
【0017】本発明の半導体装置の製造方法において、前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、好ましくは、前記ポリシリコン膜の不純物がドーピングされた部分をエッチングする際における前記側壁保護膜の膜厚を、前記ポリシリコン膜の不純物がドーピングされていないポリシリコン膜をエッチングする際における前記側壁保護膜の膜厚よりも厚くしながらエッチングする工程である。
【0018】また、本発明の半導体装置の製造方法にお

いては、前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、より好ましくは、前記ポリシリコン膜の不純物がドーピングされた部分をエッチングする際における前記側壁保護膜形成用のガス量を、前記ポリシリコン膜の不純物がドーピングされていない部分をエッチングする際における前記側壁保護膜形成用ガス量よりも多く用いてエッチングする工程である。

【0019】前記側壁保護膜形成用のガスは、好ましくは、臭化水素又はヨウ化水素であり、前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、好ましくは、反応性イオンエッチング（Reactive Ion Etching）であり、前記側壁保護膜の膜厚を変化させてドライエッチングを行う工程は、エッチング用ガスとして、塩素、酸素および臭化水素を含有するガスが好ましい。

【0020】本発明の製造方法は、好適には、ＭＯＳ型トランジスタを有する半導体装置の製造方法であって、半導体基板上に絶縁膜を形成する工程と、該絶縁膜上にポリシリコンからなる層を形成する工程と、該ポリシリコンからなる層に不純物をドーピングする工程と、前記ポリシリコンからなる層の不純物がドーピングされた部分を、側壁保護膜の膜厚が厚い状態でドライエッチングを行う工程と、前記ポリシリコンからなる層の不純物がドーピングされていない部分を側壁保護膜が薄い状態でドライエッチングを行う工程とを有する。

【0021】

【発明の実施の形態】次に、本発明の実施の形態により、本発明の半導体装置の製造方法を詳細に説明する。

【0022】<u>第１実施形態</u>

本発明の第１の実施形態は、本発明の半導体製造方法を用いるＭＯＳ型トランジスタのゲート電極の形成方法、すなわち、前記素子形成層がゲート電極の場合の適用例である。

【0023】先ず、図１（ａ）に示すように、例えば、シリコン半導体基板等の半導体基板１上に、酸化シリコン等の酸化絶縁膜２を、例えば、熱ＣＶＤ法、ＬＯＣＯＳ酸化等の通常の方法により形成する。この場合、Ｎチャネル MＯＳトランジスタを形成する場合にはｐ型シリコン半導体基板を、ＰチャネルＭＯＳトランジスタを形成する場合には、ｎ型シリコン半導体基板を用いる。

【0024】次いで、該酸化絶縁膜上に、例えば、ＣＶＤ法等の通常の方法により、ポリシリコン膜３を全面に形成する。

【0025】次に、図１（ｂ）に示すように、前記ポリシリコン膜３表層部に、例えば、イオン注入法により、不純物をイオン注入する。不純物としては、ｎ型不純物としてリンや砒素の化合物を、ｐ型不純物としてホウ素化合物を用いることができる。このイオン注入により、ポリシリコン膜３表層部分には、リンや砒素等のｎ型不純物がドープされた部分４が形成される。

【0026】次いで、図１（ｃ）に示すように、全面に酸化シリコン膜５を、例えば、ＣＶＤ法等により堆積させる。次に、図２（ｄ）に示すように、全面に図示しないレジスト膜を堆積させ、例えば、フォトエッチングにより電極形成のための酸化シリコン膜５のパターニングを行う。

【0027】このようにして得られた基板に対して、ポリシリコン膜３を、次のような条件で、側壁保護膜を用いる反応性イオンエッチング（Reactive Ion Etching）等のドライエッチングにより、ゲート電極のパターン形成を行う。

【0028】先ず、図示しないポリシリコン膜３の表層部の自然酸化膜をエッチングにより除去する。このときのエッチング条件は、例えば、以下のようである。

【0029】

エッチングガス流量：Cl_2 １２０ｓｃｃｍ
温度　：２０℃
マイクロ波（２．４５ＧＨｚ）出力：４００Ｗ
基板バイアス高周波（４００ｋＨｚ）出力：５０Ｗ
排気量　：６００l／ｓ

続いて、図２（ｅ）に示すように、ポリシリコン膜３の表層部の不純物がドープされた部分を、例えば、塩素ガスと酸素ガスの混合ガス等のドライエッチング用ガスと、例えば、臭化水素等の側壁保護膜形成用のガスを併用することにより、ドライエッチングを行う。このときのドライエッチング条件は、例えば、以下のようである。

【0030】

ガス流量：Cl_2 ６０ｓｃｃｍ
O_2 ５ｓｃｃｍ
ＨＢｒ６０ｓｃｃｍ
温度　：２０℃
マイクロ波（２．４５ＧＨｚ）出力：４００Ｗ
基板バイアス高周波（４００ｋＨｚ）出力：２５Ｗ
排気量　：３００l／ｓ

この場合、不純物濃度は表層ほど高く、また不純物濃度が高い程、エッチングレートも高くなるため、エッチング後のポリシリコン膜３の表層部の形状は、ポリシリコン膜３の表層部から下に向かう程ゲートの幅が拡がっているのが通常である。

【0031】次に、図２（ｆ）に示すように、ポリシリコン膜３の下層部の不純物がドープされていない部分を、例えば、塩素ガスと酸素ガスの混合ガス等のドライエッチング用ガスと、例えば、臭化水素等の側壁保護膜形成用のガスを併用してドライエッチングを行う。このときのドライエッチングの条件は、例えば、以下の条件である。

【0032】

ガス流量：Cl_2 90sccm
　　　　　O_2　5sccm
　　　　　HBr30sccm

温度　　：20℃
マイクロ波（2．45GHz）出力：400W
基板バイアス高周波（400kHz）出力：25W
排気量　：600l／s

本発明の製造方法は、ポリシリコン膜3の表層部の不純物がドープされた部分と、ポリシリコン膜3の下層部の不純物がドープされていない部分との側壁保護膜の膜厚を変化させながら、ドライエッチングを行って、ゲート電極のパターンを形成を行うことを特徴とする。すなわち、ポリシリコン膜3を側壁保護膜を用いて、ドライエッチングを行う際、ポリシリコン膜3の層中に含まれる不純物の濃度に応じて、側壁保護膜の膜厚を変化させながら、ドライエッチングを行うものである。

【0033】通常、ポリシリコン中にドープされた不純物濃度が高い程、エッチャント（エッチングガス）に対するエッチングレートが高い。従って、ポリシリコン膜3中に含まれる不純物濃度が高い部分は、側壁保護膜の膜厚を厚くし、すなわち、側壁保護膜形成用ガスの量を多くして、ドライエッチングを行い、ポリシリコン膜3中に含まれる不純物濃度が低いかあるいは存在しない部分は、側壁保護膜の膜厚を相対的に薄くし、すなわち、側壁保護膜形成用ガスの量を少なくして、ドライエッチングを行う。

【0034】側壁保護膜の膜厚は、側壁保護膜用ガスの流量、真空チャンバーから排気するガスの排気量、および試料台の温度等の各種パラメータによって、自由に設定することができる。

【0035】このように側壁保護膜の膜厚を変化させながら、ドライエッチングを行うことによって、従来問題となっていた、ポリシリコン膜中の不純物濃度が高い部分におけるサイドエッチングの発生を効果的に防止することができる。

【0036】従って、本発明の第1実施形態の半導体製造方法によれば、側壁保護膜を用いながらドライエッチングにより素子形成層を所定のパターンに形成する際に生じる、エッチングレートの相違に起因するサイドエッチングの発生を防止し、サリサイド工程により形成されるチタニウムシリサイド等の金属シリサイドの形成面積が小さくなって、いわゆる細線効果に伴う抵抗上昇を抑制して、信頼性の高い半導体装置を製造する製造方法を提供することができる。

【0037】<u>第2実施形態</u>
本発明の第2実施形態は、本発明の製造方法を適用したNチャネルMOSトランジスタの製造例である。

【0038】先ず、図3（a）に示すように、p型シリコン半導体基板6上に、LOCOS法（Locos Oxidation of Silicon）により、膜厚の厚い酸化シリコン膜（素

子分離膜）7を形成する。この場合、さらに素子形成領域上の酸化シリコン膜を一度除去し、例えば、CVD法、スパッタリング法等により、再度酸化シリコン膜（ゲート酸化膜11）を形成することもできる。

【0039】続いて、図3（b）に示すように、全面にポリシリコン層8を、例えば、CVD法またはスパッタリング法等により形成し、その表層部に、例えば、リン化合物等の周期律表の第5B族元素の化合物をイオン注入法によりイオン注入することにより、ポリシリコン層8の表層部に不純物がドープされた部分9を形成する。

【0040】次に、図3（c）に示すように、全面に酸化シリコン膜10を、例えば、CVD法により形成する。次いで、図4（d）に示すように、図示しないレジスト膜を全面に堆積させたのち、フォトエッチングによりパターニングを行い、エッチングのより酸化シリコン膜10を所定のパターンに形成する。

【0041】次いで、ポリシリコン膜8を、第1実施形態の場合と同様に、ポリシリコン膜3の表層部の不純物がドープされた部分と、ポリシリコン膜8の下層部の不純物がドープされていない部分との側壁保護膜の膜厚を変化させながら、ドライエッチングを行って、ゲート電極のパターンを形成を行う。ポリシリコン膜8の表層部の不純物がドープされた部分をドライエッチングしたときの途中図を図4（e）に、ポリシリコン膜8の下層部の不純物がドープされていない部分をドライエッチングして、ゲート電極を形成した状態を図4（f）にそれぞれ示す。

【0042】このように、第1実施形態と同様にして側壁保護膜の膜厚を変化させながら、ドライエッチングを行うことによって、従来問題となっていたポリシリコン膜中の不純物濃度が高い部分におけるサイドエッチングの発生を有効に防止することができる。

【0043】次いで、図5（g）に示すように、ゲート電極下部のゲート酸化膜11を残し、基板6上の素子領域の酸化シリコン膜をエッチング除去したのち、リンや砒素等のn型不純物を、ゲート電極と素子分離膜との間に、例えば、イオン注入法により、比較的浅くイオン注入を行うことにより、低濃度の不純物がドープされたn^-領域12を形成する。このときのイオン注入の条件は、例えば、10〜30keVのエネルギー、2×10^{13}〜8×10^{13}／cm^2 のドーズ量である。

【0044】次に、図5（h）に示すように、全面に酸化シリコン等の酸化絶縁膜を堆積させたのち、異方性エッチングにより、前記ゲート電極側面にサイドウォール14を形成して、前記n^-領域12の更に外側で、サイドウォール14のエッジド方から外側にかけて、例えば、イオン注入法により、比較的深くイオン注入を行うことにより、高濃度の不純物がドープされたn^+領域13を形成する。このときのイオン注入の条件は、例えば、40〜80keVのエネルギー、1×10^{14}〜8×

$10^{15}/cm^2$ のドーズ量である。

【0045】このようにして形成される構造は、LDD構造（Lightly Doped Drain Structure ）といわれており、いわゆるホットエレクトロン効果を低減するために設けられる。

【0046】次いで、図5（i）に示すように、ゲート電極上層の酸化シリコン膜を、エッチングにより除去し、図6（j）に示すように、チタニウム層を、例えば、スパッタリング法等により、全面に堆積させたのち、加熱することによって、ポリシリコン膜上のチタニウムをチタニウムシリサイドとしたのち、未反応のチタニウムのみを除去することにより、導電性の高いチタニウムシリサイド膜15をシリコン膜上に形成する。

【0047】そして、図6（k）に示すように、全面に層間絶縁膜16を形成する。その後は、コンタクトホールを形成し、所定の配線構造等を形成することにより、目的とするNチャネルMOSトランジスタを有する半導体装置を製造することができる。

【0048】第2実施形態の半導体製造方法によれば、第1実施形態と同様、側壁保護膜を用いながらドライエッチングにより素子形成層を所定のパターンに形成する際に生じる、エッチングレートの相違に起因するサイドエッチングの発生を防止し、サリサイド工程により形成されるチタニウムシリサイド等の金属シリサイドの形成面積が小さくなって、いわゆる細線効果に伴う抵抗上昇を抑制して、信頼性の高い半導体装置を製造する製造方法を製造することができる。

【0049】なお、上記実施の形態では、ゲート電極の形成を例にとり、本発明を説明したが、本発明の半導体製造方法は、RIE等のドライエッチング法において、例えば、不純物がドープされた層とドープされていない層の場合のように、エッチャントに対するエッチングレートの相違に起因する局所的なサイドエッチングの発生を効果的に防止できることを特徴とする。従って、広く一般的な素子形成層の加工において、エッチャントに対するエッチングレートの相違に起因する局所的なサイドエッチングが生じる場合にも適用することができるのはいうまでもない。

【0050】

【発明の効果】以上説明したように、本発明は、ゲート電極等の素子形成層を側壁保護膜を用いて所定のパターンに形成するためのドライエッチング工程を有する半導体装置の製造方法であって、前記ドライエッチング工程は、側壁保護膜の膜質を変化させてドライエッチングを行う工程である半導体装置の製造方法である。

【0051】本発明によれば、側壁保護膜を用いながらドライエッチングにより素子形成層を所定のパターンに形成する際に生じる、エッチングレートの相違に起因するサイドエッチングの発生を防止することができ、かつ、寸法の太りが少ない素子形成層のドライエッチングが可能となる。

【0052】従って、引き続くサリサイド工程により形成されるチタニウムシリサイド等の金属シリサイドの形成面積が小さくなって、いわゆる細線効果に伴う抵抗上昇を抑制することができ、信頼性の高い微細構造を有する半導体装置を製造することができる。

【図面の簡単な説明】

【図1】図1は、本発明の第1実施形態の半導体装置の製造の各工程の概要を示す図である。（a）は、半導体基板上に絶縁膜とポリシリコン膜を形成した断面図であり、（b）は、（a）に示す状態から、ポリシリコン膜表層部に不純物をイオン注入した断面図であり、（c）は、さらにその上に酸化シリコン膜を形成した状態の断面図である。

【図2】図2は、本発明の第1実施形態の半導体装置の製造の各工程の概要を示す図である。（d）は、図1（c）に示す状態から、酸化シリコン膜を加工した断面図であり、（e）は、（d）に示す状態から、ポリシリコン膜表層部の不純物が含有されている部分をドライエッチングした途中の断面図であり、（f）は、（e）に示す状態から、ポリシリコン膜の不純物を含有しない部分をドライエッチングしてゲート電極を形成した断面図である。

【図3】図3は、本発明の第2実施形態の半導体装置の製造の各工程の概要を示す図である。（a）は、p型シリコン半導体基板上にLOCOS法により、素子分離を行った断面図であり、（b）は、全面にポリシリコン膜を形成し、その表層にn型不純物をイオン注入した断面図であり、（c）は、さらにポリシリコン膜の上に酸化シリコン膜を形成した断面図である。

【図4】図4は、本発明の第2実施形態の半導体装置の製造の各工程の概要を示す図である。（d）は、図3（c）に示す状態から、酸化シリコン膜を加工した断面図であり、（e）は、（d）に示す状態から、ポリシリコン膜表層部の不純物が含有されている部分をドライエッチングした途中の断面図であり、（f）は、（e）に示す状態から、ポリシリコン膜の不純物を含有しない部分をドライエッチングしてゲート電極を形成した断面図である。

【図5】図5は、本発明の第2実施形態の半導体装置の製造の各工程の概要を示す図である。（g）は、図4（f）に示す状態から、ゲート電極エッジ部と素子分離膜との間に存在する酸化シリコン膜を除去し、そこへ、n型不純物をイオン注入して、n^- 領域を形成した断面図であり、（h）は、（g）に示す状態から、サイドウォールを形成したのち、サイドウォールエッジ部と素子分離膜との間にn型不純物をイオン注入して、n^+ 領域を形成した図であり、（i）は、（h）に示す状態から、ゲート電極上の酸化シリコン膜をエッチングにより除去した断面図である。

【図6】図6は、本発明の第2実施形態の半導体装置の製造の各工程の概要を示す図である。（j）は、図5（i）に示す状態から、シリコン上にチタニウムシリサイド膜を形成した断面図であり、（k）は、（j）に示す状態から、層間絶縁膜を全面に形成した図である。

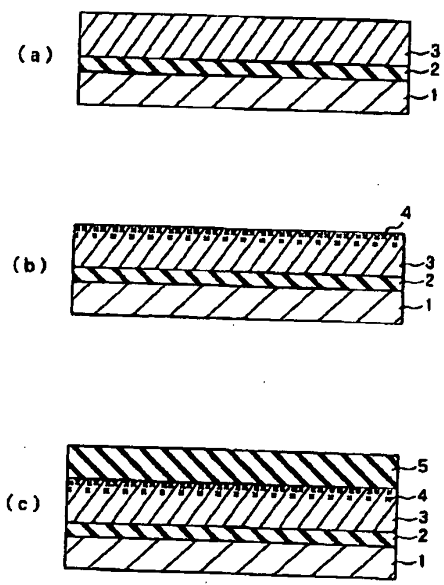
【図7】図7は、従来のドライエッチング法によるゲート電極の形成方法の各工程を示す図である。（a）は、半導体基板上に、絶縁膜を介してポリシリコン膜を形成し、その表層部に不純物をイオン注入したのち、酸化シリコン膜を形成し、所定のエッチングにより所定の加工を行った断面図であり、（b）は、その後、ポリシリコン膜をドライエッチングしてゲート電極を形成した断面図であり、（c）は、ゲート電極周辺部の絶縁膜を除去したのち、サイドウォールを形成した断面図である。

【図8】図8は、従来のドライエッチング法によるゲート電極の形成方法の各工程を示す図である。（d）は、図7（c）に示す状態から、ゲート電極上の酸化シリコン膜をエッチングにより除去した断面図であり、（e）は、（d）に示す状態から、シリコン上にチタニウムシリサイド膜を形成した断面図である。

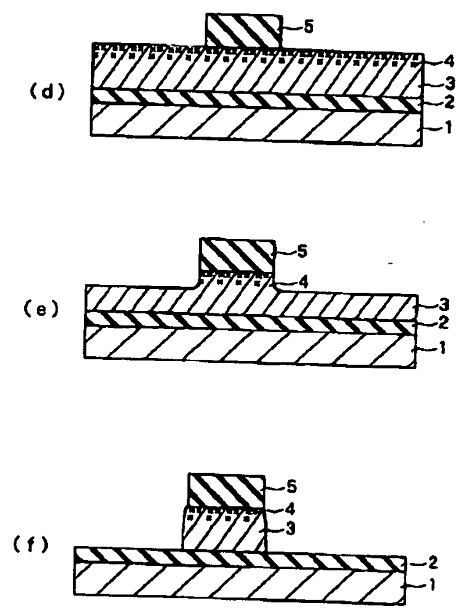
【符号の説明】

1，16…半導体基板、2，17…絶縁膜、3，8，18…ポリシリコン層、4，19…不純物、5，10，20…酸化シリコン膜、6…p型シリコン半導体基板、7…素子分離膜、9…n型不純物、11，21…ゲート酸化膜、12…n 領域、13…n^+ 領域、14，22…サイドウォール、15，23…チタニウムシリサイド、16…層間絶縁膜

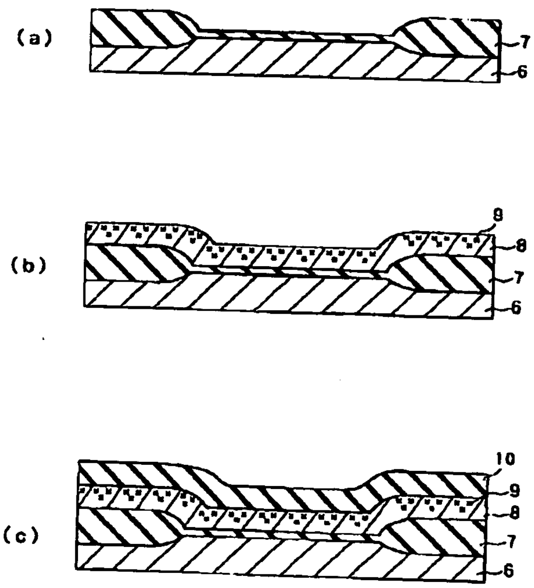
【図1】



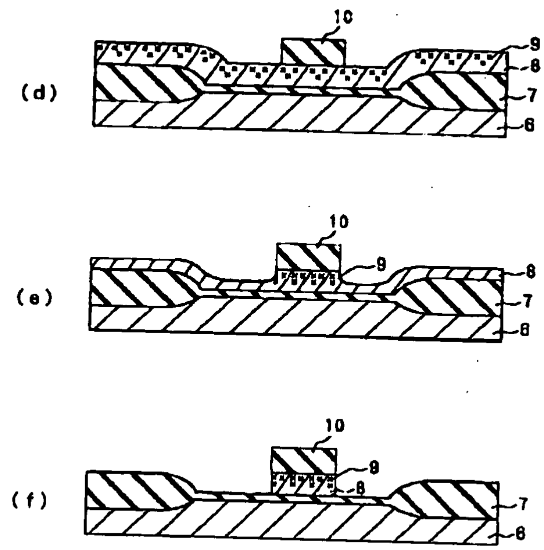
【図2】



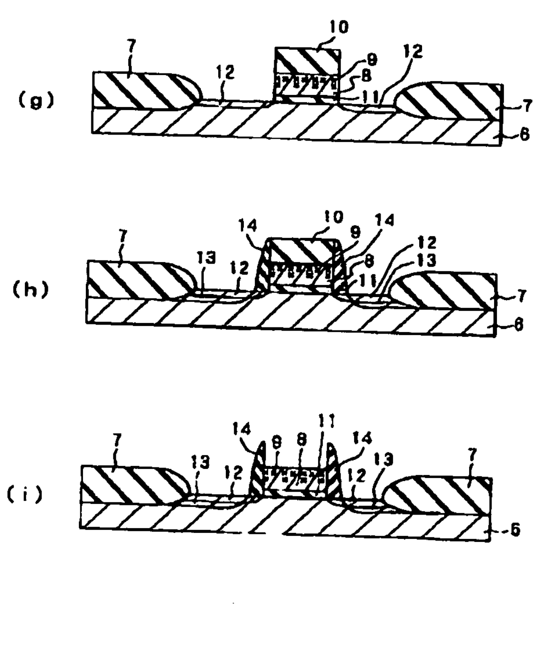
【図3】


(a)
(b)
(c)
6
7
8
9
10

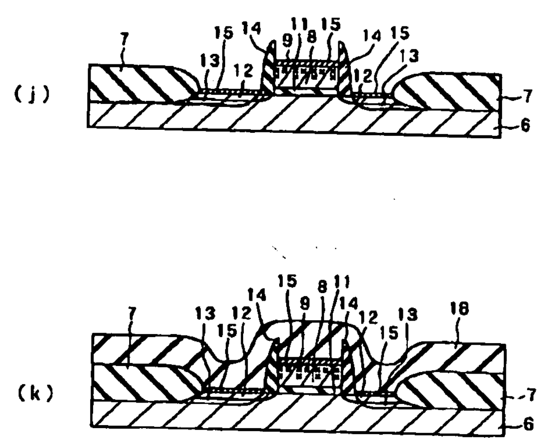
【図4】


(d)
(e)
(f)
6
7
8
9
10

【図5】

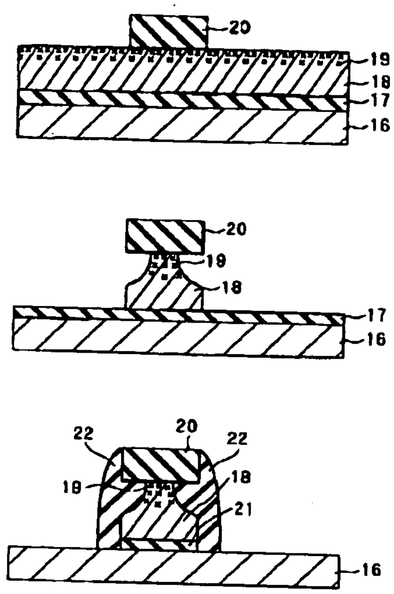

(g)
(h)
(i)
6
7
8
9
10
11
12
13
14

【図6】


(j)
(k)
6
7
8
9
11
12
13
14
15
16

【図7】

(a)
(b)
(c)


20
19
18
17
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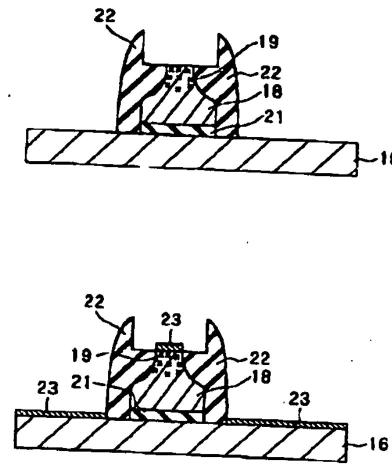
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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] It is the manufacture approach of a semiconductor device which is the process which said dry etching process changes the thickness of a side-attachment-wall protective coat in the manufacture approach of a semiconductor device of having a dry etching process for forming the component formative layer in a predetermined pattern using a side-attachment-wall protective coat, and performs dry etching.
[Claim 2] The process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is the manufacture approach of a semiconductor device according to claim 1 which consists of a process to which the thickness of a side-attachment-wall protective coat carries out dry etching in the thick condition, and a process to which the thickness of a side-attachment-wall protective coat carries out dry etching in the thin condition.
[Claim 3] The process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is the manufacture approach of a semiconductor device according to claim 1 which is the process which performs dry etching while changing the thickness of a side-attachment-wall protective coat according to the etching rate to etching gas.
[Claim 4] The process to which the thickness of said side-attachment-wall protective coat carries out dry etching in the thick condition is a manufacturing method of a semiconductor device according to claim 1 which is the process which etches the polish recon film with which the impurity was doped.
[Claim 5] The dry etching process for forming a predetermined pattern, forming said side-attachment-wall protective coat is the manufacture approach of a semiconductor device according to claim 1 which is the process which forms a gate electrode.
[Claim 6] Said impurity is a manufacturing method of a semiconductor device according to claim 4 which is 5B group element of the periodic table.
[Claim 7] The process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is a manufacturing method of a semiconductor device according to claim 1 which is the process etched while making it thicker than the thickness of said side-attachment-wall protective coat at the time of etching the polish recon film with which the impurity of said polish recon film is not doped in the thickness of said side-attachment-wall protective coat at the time of etching the part by which the impurity of said polish recon film was doped.
[Claim 8] The process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is a manufacturing method of a semiconductor device according to claim 1 which is the process which uses and is etched rather than said capacity for side-attachment-wall protective coat formation at the time of etching the part by which the impurity of said polish recon film is not doped in the capacity for said side-attachment-wall protective coat formation at the time of etching the part by which the impurity of said polish recon film was doped. [many]
[Claim 9] The gas for said side-attachment-wall protective coat formation is a manufacturing method of a semiconductor device according to claim 8 which is a hydrogen bromide.
[Claim 10] The process which the thickness of said side-attachment-wall protective coat is changed, and

performs dry etching is a manufacturing method of a semiconductor device according to claim 1 which is reactive ion etching (Reactive Ion Etching).

[Claim 11] The process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is a manufacturing method of a semiconductor device according to claim 1 which is a process using the gas containing chlorine, oxygen, and a hydrogen bromide as gas for etching.

[Claim 12] The process which forms an insulator layer on a semi-conductor substrate, and the process which forms the layer which consists of polish recon on this insulator layer, The process which dopes an impurity in the layer which consists of this polish recon, and the process to which the thickness of a side-attachment-wall protective coat carries out dry etching for the part by which the impurity of the layer which consists of said polish recon was doped in the thick condition, The manufacture approach of a semiconductor device of having the process which performs dry etching for the part by which the impurity of the layer which consists of said polish recon is not doped in the condition that a side-attachment-wall protective coat is thin.

[Claim 13] Said impurity is a manufacturing method of a semiconductor device according to claim 12 which is 5B group element of the periodic table.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device, especially the dry etching approach used in the gate electrode formation process of an MOS (Metal Oxide Semiconductor) transistor.
[0002]
[Description of the Prior Art] In recent years, in the field of a semiconductor device, integration advances increasingly, for example, detailed-ization of the structure progresses about a VLSI, and the demand to ultra-fine processing technology is becoming still severer. For example, development of the process which is compatible in an anisotropy and a high selection ratio is desired also about gate processing using silicon system ingredients including polish recon.
[0003] By the way, the technique of etching is taken, forming a protective coat (henceforth a "side-attachment-wall protective coat") in the side attachment wall of a layer, when the resultant which generated ingredients other than an oxide film about reservation of the anisotropy configuration by plasma etching at the time of plasma etching when for example, the component formative layer was formed by the predetermined pattern re-dissociates in the plasma.
[0004] Moreover, the absolute value and dispersion of dimension gaps, such as the component formative layer, have posed a problem with detailed-izing of the structure of the latest semiconductor device. The approach of shortening the residence time of the etching gas under etching processing has been adopted by etching as a cure for it, performing for example, high-speed exhaust air.
[0005] However, by the above-mentioned approach, as a result of the residence time of the etching gas under etching processing becoming short, it is controlled that a resultant re-dissociates in the plasma during etching processing, deposits decrease in number, and a side-attachment-wall protective coat thin-film-izes. If a side-attachment-wall protective coat thin-film-izes, side etching will progress too much, or the phenomenon called notching will arise, and the absolute value and the problem of dispersion of dimension gaps, such as the component formative layer, will not be solved.
[0006] Although there is also a method of raising substrate impression bias as a cure for this, there are a fall of the selection ratio to etching with the gate oxide of a substrate and fear of oxide-film degradation by plasma damage generating shortly.
[0007] On the other hand, in the semiconductor device, when using the polish recon film as an electrode material or a contact ingredient, after growing up the polish recon film, it is usually heat-treating by doping impurities, such as Lynn and boron, in polish recon by ion-implantation or the diffusion method by chemical vapor deposition (CVD method) or the sputtering method. Thus, when the polish recon film containing an impurity is used as a gate electrode on gate oxide, by heat treatment added after polish recon film growth, an impurity is spread in gate oxide and degradation is brought to the membraneous quality.
[0008] In order to avoid it, the technique of performing processing of a gate electrode, i.e., the dry etching of the polish recon film containing an impurity, is known without heat-treating.

[0009]
[Problem(s) to be Solved by the Invention] However, by the technique of not performing the above-mentioned heat treatment, the doped impurity will incline and exist in the polish recon surface section. The part which doped n mold dopant which are periodic table 5B group elements, such as Lynn and arsenic Since the etching rate (etched easy) is large as compared with the polish recon which is not doped, there is a problem on which side etching goes into the surface section of the polish recon film with which n mold impurity was doped locally (refer to drawing 7 R> 7 (a) and (b)). In addition to the thinness of the side-attachment-wall protective coat by the above high-speed exhaust air processes, such side etching originates in accelerating of the etching rate produced in n mold doped polysilicon.
[0010] When side etching occurs, the silicon nitride film excellent in step coverage nature for sidewall spacer formation will enter into this side etching section, and a gate electrode top face will be covered in the side etching section (refer to drawing 7 (c) and drawing 8 (d), and (e)).
[0011] Therefore, the formation area of metal silicide, such as titanium silicide formed of the next Salicide process, becomes small, the resistance rise accompanying the so-called thin line effectiveness is brought about, and there is a possibility of leading to the fall of the dependability of a semiconductor device.
[0012] Generating of side etching resulting from the difference of the etching rate produced in case the component formative layer is formed in a predetermined pattern by dry etching, using a side-attachment-wall protective coat is prevented, the formation area of metal silicide, such as titanium silicide formed of the Salicide process, becomes small, this invention controls the resistance rise accompanying the so-called thin line effectiveness, and it aims at offering the manufacture approach of manufacturing a reliable semiconductor device.
[0013]
[Means for Solving the Problem] This invention is the manufacture approach of a semiconductor device of having a dry etching process for forming the component formative layer in a predetermined pattern using a side-attachment-wall protective coat this purpose being attained, and said dry etching process offers the manufacture approach of the semiconductor device which is the process which the thickness of a side-attachment-wall protective coat is changed, and performs dry etching.
[0014] In the manufacture approach of the semiconductor device of this invention, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is the manufacture approach of the semiconductor device which consists of a process to which the thickness of a side-attachment-wall protective coat carries out dry etching in the thick condition preferably, and a process to which the thickness of a side-attachment-wall protective coat carries out dry etching in the thin condition.
[0015] In the manufacture approach of the semiconductor device of this invention, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is the manufacture approach of the semiconductor device which is the process which performs dry etching preferably while changing the thickness of a side-attachment-wall protective coat according to the etching rate to etching gas.
[0016] In the manufacture approach of the semiconductor device of this invention, the process to which the thickness of said side-attachment-wall protective coat carries out dry etching in the thick condition is a process which etches the polish recon film with which the impurity was doped preferably, the dry etching process for forming a predetermined pattern, forming said side-attachment-wall protective coat is a process which forms a gate electrode, and said impurity has desirable 5B group element of the periodic table.
[0017] The process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching in the manufacture approach of the semiconductor device of this invention is a process etched while making it thicker than the thickness of said side-attachment-wall protective coat at the time of etching the polish recon film with which the impurity of said polish recon film is not doped in the thickness of said side-attachment-wall protective coat at the time of etching preferably the part by which the impurity of said polish recon film was doped.

[0018] Moreover, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching in the manufacture approach of the semiconductor device of this invention is a process which uses and is etched rather than said capacity for side-attachment-wall protective coat formation at the time of etching the part by which the impurity of said polish recon film is not doped in the capacity for said side-attachment-wall protective coat formation at the time of etching more preferably the part by which the impurity of said polish recon film was doped. [many]
[0019] The gas for said side-attachment-wall protective coat formation is a hydrogen bromide or hydrogen iodide preferably, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is reactive ion etching (Reactive Ion Etching) preferably, and the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching has desirable gas containing chlorine, oxygen, and a hydrogen bromide as gas for etching.
[0020] The process which the manufacture approach of this invention is the manufacture approach of a semiconductor device of having a MOS transistor, suitably, and forms an insulator layer on a semi-conductor substrate, The process which forms the layer which consists of polish recon on this insulator layer, and the process which dopes an impurity in the layer which consists of this polish recon, The process to which the thickness of a side-attachment-wall protective coat carries out dry etching for the part by which the impurity of the layer which consists of said polish recon was doped in the thick condition, It has the process which performs dry etching for the part by which the impurity of the layer which consists of said polish recon is not doped in the condition that a side-attachment-wall protective coat is thin.
[0021]
[Embodiment of the Invention] Next, the gestalt of operation of this invention explains the manufacture approach of the semiconductor device of this invention to a detail.
[0022] The 1st operation gestalt of 1st operation gestalt this invention is an example of application in case the formation approach of the gate electrode of the MOS transistor which uses the semi-conductor manufacture approach of this invention, i.e., said component formative layer, is a gate electrode.
[0023] First, as shown in drawing 1 (a), the oxidation insulator layers 2, such as silicon oxide, are formed by the usual approaches, such as for example, a heat CVD method and LOCOS oxidation, on the semi-conductor substrates 1, such as a silicon semi-conductor substrate. In this case, in forming an N-channel metal oxide semiconductor transistor and forming a P channel MOS transistor for a p-type silicon semi-conductor substrate, it uses n mold silicon semi-conductor substrate.
[0024] Subsequently, the polish recon film 3 is formed by the usual approaches, such as a CVD method, on this oxidation insulator layer on the whole surface.
[0025] Next, as shown in drawing 1 (b), the ion implantation of the impurity is carried out to said polish recon film 3 surface section with ion-implantation. As an impurity, the compound of Lynn or arsenic can be used as an n mold impurity, and a boron compound can be used as a p mold impurity. Of this ion implantation, the part 4 by which n mold impurities, such as Lynn and arsenic, were doped is formed in a polish recon film 3 surface part.
[0026] Subsequently, the silicon oxide film 5 is made to deposit on the whole surface with a CVD method etc., as shown in drawing 1 (c). Next, as shown in drawing 2 (d), the resist film which is not illustrated on the whole surface is made to deposit, for example, photo etching performs patterning of the silicon oxide film 5 for electrode formation.
[0027] Thus, dry etching, such as reactive ion etching [film / 3 / polish recon] (Reactive Ion Etching) using a side-attachment-wall protective coat, performs pattern formation of a gate electrode on the following conditions to the obtained substrate.
[0028] First, etching removes the natural oxidation film of the surface section of the polish recon film 3 which is not illustrated. The etching conditions at this time are as follows, for example.
[0029]
Etching gas flow rate : Cl2 120sccm temperature : 20-degree-C microwave (2.45GHz) output: -- 400W substrate bias RF (400kHz) output: -- 50W displacement As shown in 600l. /, then drawing 2 (e) s, the part by which the impurity of the surface section of the polish recon film 3 was doped : For example,

chlorine gas and dry etching gases, such as mixed gas of oxygen gas, For example, dry etching is performed by using together the gas for side-attachment-wall protective coat formation of a hydrogen bromide etc. The dry etching conditions at this time are as follows, for example.

[0030]

ガス流量：Cl_2 60sccm
O_2 5sccm
HBr60sccm

temperature : -- 20-degree-C microwave (2.45GHz) output: -- 400W substrate bias RF (400kHz) output: -- 25W displacement : Since an etching rate also becomes high so that high impurity concentration is as high as a surface in this case 300l./s and high impurity concentration is high, it usually comes out of it that the width of face of the gate has spread, so that the configuration of the surface section of the polish recon film 3 after etching goes downward from the surface section of the polish recon film 3.

[0031] Next, as shown in drawing 2 (f), for example, chlorine gas, dry etching gases, such as mixed gas of oxygen gas, and the gas for side-attachment-wall protective coat formation of a hydrogen bromide etc. are used together for the part by which the impurity of the lower layer section of the polish recon film 3 is not doped, and dry etching is performed. The conditions of the dry etching at this time are the following conditions.

[0032]

ガス流量：Cl_2 90sccm
O_2 5sccm
HBr30sccm

temperature : -- 20-degree-C microwave (2.45GHz) output: -- 400W substrate bias RF (400kHz) output: -- 25W displacement : The manufacture approach of 600l. [/] this invention s It is characterized by performing dry etching and forming the pattern of a gate electrode, changing the thickness of the side-attachment-wall protective coat of the part by which the impurity of the surface section of the polish recon film 3 was doped, and the part by which the impurity of the lower layer section of the polish recon film 3 is not doped. That is, dry etching is performed, changing the thickness of a side-attachment-wall protective coat according to the concentration of the impurity contained in the layer of the polish recon film 3 in the polish recon film 3 in case dry etching is performed using a side-attachment-wall protective coat.

[0033] Usually, the etching rate to etchant (etching gas) is so high that the high impurity concentration doped in polish recon is high. or [therefore, / that the part with the high high impurity concentration contained in the polish recon film 3 has the low high impurity concentration which thickens thickness of a side-attachment-wall protective coat, namely, makes / many / the amount of the gas for side-attachment-wall protective coat formation, performs dry etching, and is contained in the polish recon film 3] -- or the part not existing makes thin relatively thickness of a side-attachment-wall protective coat, namely, lessens the amount of the gas for side-attachment-wall protective coat formation, and performs dry etching.

[0034] The thickness of a side-attachment-wall protective coat can be freely set up with various parameters, such as a flow rate of the gas for side-attachment-wall protective coats, displacement of the gas exhausted from a vacuum chamber, and temperature of a sample base.

[0035] Thus, generating of side etching in a part with the high high impurity concentration in the polish recon film which had become a problem conventionally can be effectively prevented by performing dry etching, changing the thickness of a side-attachment-wall protective coat.

[0036] Therefore, in case the component formative layer is formed in a predetermined pattern by dry etching according to the semi-conductor manufacture approach of the 1st operation gestalt of this invention, using a side-attachment-wall protective coat, are generated. Prevent generating of side etching resulting from the difference of an etching rate, the formation area of metal silicide, such as titanium

silicide formed of the Salicide process, becomes small, and the resistance rise accompanying the so-called thin line effectiveness is controlled. The manufacture approach of manufacturing a reliable semiconductor device can be offered.

[0037] The 2nd operation gestalt of 2nd operation gestalt this invention is the example of manufacture of the N-channel metal oxide semiconductor transistor which applied the manufacture approach of this invention.

[0038] first, it is shown in drawing 3 (a) -- as -- the p-type silicon semi-conductor substrate 6 top -- LOCOS -- law (Locos Oxidation of Silicon) The thick silicon oxide film (component demarcation membrane) 7 of thickness is formed. In this case, the silicon oxide film on a component formation field can be removed further once, for example, the silicon oxide film (gate oxide 11) can also be again formed by the CVD method, the sputtering method, etc.

[0039] then, it is shown in drawing 3 (b) -- as -- the whole surface -- the polish recon layer 8 -- for example, a CVD method or the sputtering method etc. -- forming -- the surface section -- the [for example, / of the periodic tables, such as phosphorus compounds,] -- the part 9 in which the impurity was doped by the surface section of the polish recon layer 8 is formed by carrying out the ion implantation of the compound of 5B group element with ion-implantation.

[0040] Next, as shown in drawing 3 (c), the silicon oxide film 10 is formed in the whole surface with a CVD method. Subsequently, after making the resist film which is not illustrated deposit on the whole surface as shown in drawing 4 (d), photo etching performs patterning and the silicon oxide film 10 is formed in a predetermined pattern from that of etching.

[0041] Subsequently, changing the thickness of the side-attachment-wall protective coat of the part by which the impurity of the surface section of the polish recon film 3 was doped like the case of the 1st operation gestalt in the polish recon film 8, and the part by which the impurity of the lower layer section of the polish recon film 8 is not doped, dry etching is performed and the pattern of a gate electrode is formed. Dry etching of the part in which the impurity of the lower layer section of the polish recon film 8 is not doped in the Fig. by drawing 4 (e) is carried out the middle when carrying out dry etching of the part by which the impurity of the surface section of the polish recon film 8 was doped, and the condition of having formed the gate electrode is shown in drawing 4 (f), respectively.

[0042] Thus, generating of side etching in a part with the high high impurity concentration in the polish recon film which had become a problem conventionally can be effectively prevented by performing dry etching, changing the thickness of a side-attachment-wall protective coat like the 1st operation gestalt.

[0043] Subsequently, n by which the low-concentration impurity was doped by performing an ion implantation comparatively shallowly with ion-implantation between the gate electrode and the component demarcation membrane in n mold impurities, such as Lynn and arsenic, after leaving the gate oxide 11 of the gate electrode lower part and carrying out etching removal of the silicon oxide film of the component field on a substrate 6, as shown in drawing 5 (g) - A field 12 is formed. The conditions of the ion implantation at this time are the energy of 10-30keV, and 2x1015 to 8x1015-/cm2. It is a dose.

[0044] Next, after making oxidization insulator layers, such as silicon oxide, deposit on the whole surface as shown in drawing 5 (h), a sidewall 14 is formed in said gate electrode side face by anisotropic etching, and it is said n. - n+ by which the high-concentration impurity was doped by [of a field 12] applying outside from the edge lower part of a sidewall 14, for example, outside performing an ion implantation comparatively deeply with ion-implantation further A field 13 is formed. The conditions of the ion implantation at this time are the energy of 40-80keV, and 1x1014 to 8x1014-/cm2. It is a dose.

[0045] Thus, the structure formed is called LDD structure (Lightly Doped Drain Structure), and it is established in order to reduce the so-called hot electron effectiveness.

[0046] Subsequently, as are shown in drawing 5 (i), and etching removes the silicon oxide film of the gate electrode upper layer and it is shown in drawing 6 (j) A titanium layer by the sputtering method etc., after making it deposit on the whole surface, for example, by heating After making the titanium on the polish recon film into titanium silicide, the conductive high titanium silicide film 15 is formed on the silicon film by removing only unreacted titanium.

[0047] And as shown in drawing 6 (k), an interlayer insulation film 16 is formed in the whole surface.

The semiconductor device which has the N-channel metal oxide semiconductor transistor made into the purpose can be manufactured by forming a contact hole and forming predetermined wiring structure etc. after that.

[0048] Are generated in case the component formative layer is formed in a predetermined pattern by dry etching like the 1st operation gestalt according to the semi-conductor manufacture approach of the 2nd operation gestalt, using a side-attachment-wall protective coat. Prevent generating of side etching resulting from the difference of an etching rate, the formation area of metal silicide, such as titanium silicide formed of the Salicide process, becomes small, and the resistance rise accompanying the so-called thin line effectiveness is controlled. The manufacture approach of manufacturing a reliable semiconductor device can be manufactured.

[0049] in addition , although formation of a gate electrode be took for the example and this invention be explained with the gestalt of the above-mentioned implementation , the semi-conductor manufacture approach of this invention be characterize by the thing resulting from a difference of the etching rate to etchant for which generating of local side etching can be prevent effectively in the dry etching methods , such as RIE , like [in the case of be the layer by which the impurity be doped , and the layer which be dope] . Therefore, in processing of the large general component formative layer, it cannot be overemphasized that it can apply also when local side etching resulting from the difference of the etching rate to etchant arises.

[0050]

[Effect of the Invention] As explained above, this invention is the manufacture approach of a semiconductor device of having a dry etching process for forming the component formative layers, such as a gate electrode, in a predetermined pattern using a side-attachment-wall protective coat, and said dry etching process is the manufacture approach of the semiconductor device which is the process which the thickness of a side-attachment-wall protective coat is changed, and performs dry etching.

[0051] According to this invention, generating of side etching resulting from the difference of an etching rate produced in case the component formative layer is formed in a predetermined pattern by dry etching, using a side-attachment-wall protective coat can be prevented, and the dry etching of little component formative layer of **** of a dimension becomes possible.

[0052] Therefore, the formation area of metal silicide, such as titanium silicide formed of the continuing Salicide process, can become small, the resistance rise accompanying the so-called thin line effectiveness can be controlled, and a leading semiconductor device can be manufactured for the reliable fine structure.

[Translation done.]

* NOTICES *

TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device, especially the dry etching approach used in the gate electrode formation process of an MOS (Metal Oxide Semiconductor) transistor.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In recent years, in the field of a semiconductor device, integration advances increasingly, for example, detailed-ization of the structure progresses about a VLSI, and the demand to ultra-fine processing technology is becoming still severer. For example, development of the process which is compatible in an anisotropy and a high selection ratio is desired also about gate processing using silicon system ingredients including polish recon.
[0003] By the way, the technique of etching is taken, forming a protective coat (henceforth a "side-attachment-wall protective coat") in the side attachment wall of a layer, when the resultant which generated ingredients other than an oxide film about reservation of the anisotropy configuration by plasma etching at the time of plasma etching when for example, the component formative layer was formed by the predetermined pattern re-dissociates in the plasma.
[0004] Moreover, the absolute value and dispersion of dimension gaps, such as the component formative layer, have posed a problem with detailed-izing of the structure of the latest semiconductor device. The approach of shortening the residence time of the etching gas under etching processing has been adopted by etching as a cure for it, performing for example, high-speed exhaust air.
[0005] However, by the above-mentioned approach, as a result of the residence time of the etching gas under etching processing becoming short, it is controlled that a resultant re-dissociates in the plasma during etching processing, deposits decrease in number, and a side-attachment-wall protective coat thin-film-izes. If a side-attachment-wall protective coat thin-film-izes, side etching will progress too much, or the phenomenon called notching will arise, and the absolute value and the problem of dispersion of dimension gaps, such as the component formative layer, will not be solved.
[0006] Although there is also a method of raising substrate impression bias as a cure for this, there are a fall of the selection ratio to etching with the gate oxide of a substrate and fear of oxide-film degradation by plasma damage generating shortly.
[0007] On the other hand, in the semiconductor device, when using the polish recon film as an electrode material or a contact ingredient, after growing up the polish recon film, it is usually heat-treating by doping impurities, such as Lynn and boron, in polish recon by ion-implantation or the diffusion method by chemical vapor deposition (CVD method) or the sputtering method. Thus, when the polish recon film containing an impurity is used as a gate electrode on gate oxide, by heat treatment added after polish recon film growth, an impurity is spread in gate oxide and degradation is brought to the membraneous quality.
[0008] In order to avoid it, the technique of performing processing of a gate electrode, i.e., the dry etching of the polish recon film containing an impurity, is known without heat-treating.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, this invention is the manufacture approach of a semiconductor device of having a dry etching process for forming the component formative layers, such as a gate electrode, in a predetermined pattern using a side-attachment-wall protective coat, and said dry etching process is the manufacture approach of the semiconductor device which is the process which the thickness of a side-attachment-wall protective coat is changed, and performs dry etching.
[0051] According to this invention, generating of side etching resulting from the difference of an etching rate produced in case the component formative layer is formed in a predetermined pattern by dry etching, using a side-attachment-wall protective coat can be prevented, and the dry etching of little component formative layer of **** of a dimension becomes possible.
[0052] Therefore, the formation area of metal silicide, such as titanium silicide formed of the continuing Salicide process, can become small, the resistance rise accompanying the so-called thin line effectiveness can be controlled, and a leading semiconductor device can be manufactured for the reliable fine structure.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by the technique of not performing the above-mentioned heat treatment, the doped impurity will incline and exist in the polish recon surface section. The part which doped n mold dopant which are periodic table 5B group elements, such as Lynn and arsenic Since the etching rate (etched easy) is large as compared with the polish recon which is not doped, there is a problem on which side etching goes into the surface section of the polish recon film with which n mold impurity was doped locally (refer to drawing 7 R> 7 (a) and (b)). In addition to the thinness of the side-attachment-wall protective coat by the above high-speed exhaust air processes, such side etching originates in accelerating of the etching rate produced in n mold doped polysilicon.
[0010] When side etching occurs, the silicon nitride film excellent in step coverage nature for sidewall spacer formation will enter into this side etching section, and a gate electrode top face will be covered in the side etching section (refer to drawing 7 (c) and drawing 8 (d), and (e)).
[0011] Therefore, the formation area of metal silicide, such as titanium silicide formed of the next Salicide process, becomes small, the resistance rise accompanying the so-called thin line effectiveness is brought about, and there is a possibility of leading to the fall of the dependability of a semiconductor device.
[0012] Generating of side etching resulting from the difference of the etching rate produced in case the component formative layer is formed in a predetermined pattern by dry etching, using a side-attachment-wall protective coat is prevented, the formation area of metal silicide, such as titanium silicide formed of the Salicide process, becomes small, this invention controls the resistance rise accompanying the so-called thin line effectiveness, and it aims at offering the manufacture approach of manufacturing a reliable semiconductor device.

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MEANS

[Means for Solving the Problem] This invention is the manufacture approach of a semiconductor device of having a dry etching process for forming the component formative layer in a predetermined pattern using a side-attachment-wall protective coat this purpose being attained, and said dry etching process offers the manufacture approach of the semiconductor device which is the process which the thickness of a side-attachment-wall protective coat is changed, and performs dry etching.
[0014] In the manufacture approach of the semiconductor device of this invention, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is the manufacture approach of the semiconductor device which consists of a process to which the thickness of a side-attachment-wall protective coat carries out dry etching in the thick condition preferably, and a process to which the thickness of a side-attachment-wall protective coat carries out dry etching in the thin condition.
[0015] In the manufacture approach of the semiconductor device of this invention, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is the manufacture approach of the semiconductor device which is the process which performs dry etching preferably while changing the thickness of a side-attachment-wall protective coat according to the etching rate to etching gas.
[0016] In the manufacture approach of the semiconductor device of this invention, the process to which the thickness of said side-attachment-wall protective coat carries out dry etching in the thick condition is a process which etches the polish recon film with which the impurity was doped preferably, the dry etching process for forming a predetermined pattern, forming said side-attachment-wall protective coat is a process which forms a gate electrode, and said impurity has desirable 5B group element of the periodic table.
[0017] The process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching in the manufacture approach of the semiconductor device of this invention is a process etched while making it thicker than the thickness of said side-attachment-wall protective coat at the time of etching the polish recon film with which the impurity of said polish recon film is not doped in the thickness of said side-attachment-wall protective coat at the time of etching preferably the part by which the impurity of said polish recon film was doped.
[0018] Moreover, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching in the manufacture approach of the semiconductor device of this invention is a process which uses and is etched rather than said capacity for side-attachment-wall protective coat formation at the time of etching the part by which the impurity of said polish recon film is not doped in the capacity for said side-attachment-wall protective coat formation at the time of etching more preferably the part by which the impurity of said polish recon film was doped. [many]
[0019] The gas for said side-attachment-wall protective coat formation is a hydrogen bromide or hydrogen iodide preferably, the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry etching is reactive ion etching (Reactive Ion Etching) preferably, and the process which the thickness of said side-attachment-wall protective coat is changed, and performs dry

etching has desirable gas containing chlorine, oxygen, and a hydrogen bromide as gas for etching.
[0020] The process which the manufacture approach of this invention is the manufacture approach of a semiconductor device of having a MOS transistor, suitably, and forms an insulator layer on a semi-conductor substrate, The process which forms the layer which consists of polish recon on this insulator layer, and the process which dopes an impurity in the layer which consists of this polish recon, The process to which the thickness of a side-attachment-wall protective coat carries out dry etching for the part by which the impurity of the layer which consists of said polish recon was doped in the thick condition, It has the process which performs dry etching for the part by which the impurity of the layer which consists of said polish recon is not doped in the condition that a side-attachment-wall protective coat is thin.
[0021]
[Embodiment of the Invention] Next, the gestalt of operation of this invention explains the manufacture approach of the semiconductor device of this invention to a detail.
[0022] The 1st operation gestalt of 1st operation gestalt this invention is an example of application in case the formation approach of the gate electrode of the MOS transistor which uses the semi-conductor manufacture approach of this invention, i.e., said component formative layer, is a gate electrode.
[0023] First, as shown in drawing 1 (a), the oxidation insulator layers 2, such as silicon oxide, are formed by the usual approaches, such as for example, a heat CVD method and LOCOS oxidation, on the semi-conductor substrates 1, such as a silicon semi-conductor substrate. In this case, in forming an N-channel metal oxide semiconductor transistor and forming a P channel MOS transistor for a p-type silicon semi-conductor substrate, it uses n mold silicon semi-conductor substrate.
[0024] Subsequently, the polish recon film 3 is formed by the usual approaches, such as a CVD method, on this oxidation insulator layer on the whole surface.
[0025] Next, as shown in drawing 1 (b), the ion implantation of the impurity is carried out to said polish recon film 3 surface section with ion-implantation. As an impurity, the compound of Lynn or arsenic can be used as an n mold impurity, and a boron compound can be used as a p mold impurity. Of this ion implantation, the part 4 by which n mold impurities, such as Lynn and arsenic, were doped is formed in a polish recon film 3 surface part.
[0026] Subsequently, the silicon oxide film 5 is made to deposit on the whole surface with a CVD method etc., as shown in drawing 1 (c). Next, as shown in drawing 2 (d), the resist film which is not illustrated on the whole surface is made to deposit, for example, photo etching performs patterning of the silicon oxide film 5 for electrode formation.
[0027] Thus, dry etching, such as reactive ion etching [film / 3 / polish recon] (Reactive Ion Etching) using a side-attachment-wall protective coat, performs pattern formation of a gate electrode on the following conditions to the obtained substrate.
[0028] First, etching removes the natural oxidation film of the surface section of the polish recon film 3 which is not illustrated. The etching conditions at this time are as follows, for example.
[0029]
Etching gas flow rate : Cl2 120sccm temperature : 20-degree-C microwave (2.45GHz) output: -- 400W substrate bias RF (400kHz) output: -- 50W displacement As shown in 600l. /, then drawing 2 (e) s, the part by which the impurity of the surface section of the polish recon film 3 was doped : For example, chlorine gas and dry etching gases, such as mixed gas of oxygen gas, For example, dry etching is performed by using together the gas for side-attachment-wall protective coat formation of a hydrogen bromide etc. The dry etching conditions at this time are as follows, for example.
[0030]
ガス流量：Cl_2 60sccm
O_2 5sccm
HBr60sccm

temperature : -- 20-degree-C microwave (2.45GHz) output: -- 400W substrate bias RF (400kHz) output:

-- 25W displacement : Since an etching rate also becomes high so that high impurity concentration is as high as a surface in this case 300l./s and high impurity concentration is high, it usually comes out of it that the width of face of the gate has spread, so that the configuration of the surface section of the polish recon film 3 after etching goes downward from the surface section of the polish recon film 3.
[0031] Next, as shown in drawing 2 (f), for example, chlorine gas, dry etching gases, such as mixed gas of oxygen gas, and the gas for side-attachment-wall protective coat formation of a hydrogen bromide etc. are used together for the part by which the impurity of the lower layer section of the polish recon film 3 is not doped, and dry etching is performed. The conditions of the dry etching at this time are the following conditions.
[0032]
ガス流量：Cl_2 90sccm
O_2 5sccm
HBr 30sccm

temperature : -- 20-degree-C microwave (2.45GHz) output: -- 400W substrate bias RF (400kHz) output: -- 25W displacement : The manufacture approach of 600l. [/] this invention s It is characterized by performing dry etching and forming the pattern of a gate electrode, changing the thickness of the side-attachment-wall protective coat of the part by which the impurity of the surface section of the polish recon film 3 was doped, and the part by which the impurity of the lower layer section of the polish recon film 3 is not doped. That is, dry etching is performed, changing the thickness of a side-attachment-wall protective coat according to the concentration of the impurity contained in the layer of the polish recon film 3 in the polish recon film 3 in case dry etching is performed using a side-attachment-wall protective coat.
[0033] Usually, the etching rate to etchant (etching gas) is so high that the high impurity concentration doped in polish recon is high. or [therefore, / that the part with the high high impurity concentration contained in the polish recon film 3 has the low high impurity concentration which thickens thickness of a side-attachment-wall protective coat, namely, makes / many / the amount of the gas for side-attachment-wall protective coat formation, performs dry etching, and is contained in the polish recon film 3] -- or the part not existing makes thin relatively thickness of a side-attachment-wall protective coat, namely, lessens the amount of the gas for side-attachment-wall protective coat formation, and performs dry etching.
[0034] The thickness of a side-attachment-wall protective coat can be freely set up with various parameters, such as a flow rate of the gas for side-attachment-wall protective coats, displacement of the gas exhausted from a vacuum chamber, and temperature of a sample base.
[0035] Thus, generating of side etching in a part with the high high impurity concentration in the polish recon film which had become a problem conventionally can be effectively prevented by performing dry etching, changing the thickness of a side-attachment-wall protective coat.
[0036] Therefore, in case the component formative layer is formed in a predetermined pattern by dry etching according to the semi-conductor manufacture approach of the 1st operation gestalt of this invention, using a side-attachment-wall protective coat, are generated. Prevent generating of side etching resulting from the difference of an etching rate, the formation area of metal silicide, such as titanium silicide formed of the Salicide process, becomes small, and the resistance rise accompanying the so-called thin line effectiveness is controlled. The manufacture approach of manufacturing a reliable semiconductor device can be offered.
[0037] The 2nd operation gestalt of 2nd operation gestalt this invention is the example of manufacture of the N-channel metal oxide semiconductor transistor which applied the manufacture approach of this invention.
[0038] first, it is shown in drawing 3 (a) -- as -- the p-type silicon semi-conductor substrate 6 top -- LOCOS -- law (Locos Oxidation of Silicon) The thick silicon oxide film (component demarcation membrane) 7 of thickness is formed. In this case, the silicon oxide film on a component formation field

can be removed further once, for example, the silicon oxide film (gate oxide 11) can also be again formed by the CVD method, the sputtering method, etc.
[0039] then, it is shown in drawing 3 (b) -- as -- the whole surface -- the polish recon layer 8 -- for example, a CVD method or the sputtering method etc. -- forming -- the surface section -- the [for example, / of the periodic tables, such as phosphorus compounds,] -- the part 9 in which the impurity was doped by the surface section of the polish recon layer 8 is formed by carrying out the ion implantation of the compound of 5B group element with ion-implantation.
[0040] Next, as shown in drawing 3 (c), the silicon oxide film 10 is formed in the whole surface with a CVD method. Subsequently, after making the resist film which is not illustrated deposit on the whole surface as shown in drawing 4 (d), photo etching performs patterning and the silicon oxide film 10 is formed in a predetermined pattern from that of etching.
[0041] Subsequently, changing the thickness of the side-attachment-wall protective coat of the part by which the impurity of the surface section of the polish recon film 3 was doped like the case of the 1st operation gestalt in the polish recon film 8, and the part by which the impurity of the lower layer section of the polish recon film 8 is not doped, dry etching is performed and the pattern of a gate electrode is formed. Dry etching of the part in which the impurity of the lower layer section of the polish recon film 8 is not doped in the Fig. by drawing 4 (e) is carried out the middle when carrying out dry etching of the part by which the impurity of the surface section of the polish recon film 8 was doped, and the condition of having formed the gate electrode is shown in drawing 4 (f), respectively.
[0042] Thus, generating of side etching in a part with the high high impurity concentration in the polish recon film which had become a problem conventionally can be effectively prevented by performing dry etching, changing the thickness of a side-attachment-wall protective coat like the 1st operation gestalt.
[0043] Subsequently, n by which the low-concentration impurity was doped by performing an ion implantation comparatively shallowly with ion-implantation between the gate electrode and the component demarcation membrane in n mold impurities, such as Lynn and arsenic, after leaving the gate oxide 11 of the gate electrode lower part and carrying out etching removal of the silicon oxide film of the component field on a substrate 6, as shown in drawing 5 (g) - A field 12 is formed. The conditions of the ion implantation at this time are the energy of 10-30keV, and 2x1015 to 8x1015-/cm2. It is a dose.
[0044] Next, after making oxidization insulator layers, such as silicon oxide, deposit on the whole surface as shown in drawing 5 (h), a sidewall 14 is formed in said gate electrode side face by anisotropic etching, and it is said n. - n+ by which the high-concentration impurity was doped by [of a field 12] applying outside from the edge lower part of a sidewall 14, for example, outside performing an ion implantation comparatively deeply with ion-implantation further A field 13 is formed. The conditions of the ion implantation at this time are the energy of 40-80keV, and 1x1014 to 8x1014-/cm2. It is a dose.
[0045] Thus, the structure formed is called LDD structure (Lightly Doped Drain Structure), and it is established in order to reduce the so-called hot electron effectiveness.
[0046] Subsequently, as are shown in drawing 5 (i), and etching removes the silicon oxide film of the gate electrode upper layer and it is shown in drawing 6 (j) A titanium layer by the sputtering method etc., after making it deposit on the whole surface, for example, by heating After making the titanium on the polish recon film into titanium silicide, the conductive high titanium silicide film 15 is formed on the silicon film by removing only unreacted titanium.
[0047] And as shown in drawing 6 (k), an interlayer insulation film 16 is formed in the whole surface. The semiconductor device which has the N-channel metal oxide semiconductor transistor made into the purpose can be manufactured by forming a contact hole and forming predetermined wiring structure etc. after that.
[0048] Are generated in case the component formative layer is formed in a predetermined pattern by dry etching like the 1st operation gestalt according to the semi-conductor manufacture approach of the 2nd operation gestalt, using a side-attachment-wall protective coat. Prevent generating of side etching resulting from the difference of an etching rate, the formation area of metal silicide, such as titanium silicide formed of the Salicide process, becomes small, and the resistance rise accompanying the so-called thin line effectiveness is controlled. The manufacture approach of manufacturing a reliable

semiconductor device can be manufactured.

[0049] in addition , although formation of a gate electrode be took for the example and this invention be explained with the gestalt of the above-mentioned implementation , the semi-conductor manufacture approach of this invention be characterize by the thing resulting from a difference of the etching rate to etchant for which generating of local side etching can be prevent effectively in the dry etching methods , such as RIE , like [in the case of be the layer by which the impurity be doped , and the layer which be dope] . Therefore, in processing of the large general component formative layer, it cannot be overemphasized that it can apply also when local side etching resulting from the difference of the etching rate to etchant arises.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing 1 is drawing showing the outline of each process of manufacture of the semiconductor device of the 1st operation gestalt of this invention. (a) is the sectional view in which an insulator layer and the polish recon film were formed on the semi-conductor substrate, and is a sectional view in the condition that are the sectional view which carried out the ion implantation of the impurity to the polish recon film surface section, and (c) formed the silicon oxide film on it further from the condition which shows (b) in (a).
[Drawing 2] Drawing 2 is drawing showing the outline of each process of manufacture of the semiconductor device of the 1st operation gestalt of this invention. (d) is a sectional view in the middle of being the sectional view on which the silicon oxide film was processed, and (e) having carried out dry etching of the part which the impurity of the polish recon film surface section contains from the condition shown in (d) from the condition shown in drawing 1 (c), and (f) is the sectional view which carried out dry etching of the part which does not contain the impurity of the polish recon film, and formed the gate electrode from the condition shown in (e).
[Drawing 3] Drawing 3 is drawing showing the outline of each process of manufacture of the semiconductor device of the 2nd operation gestalt of this invention. (a) -- a p-type silicon semi-conductor substrate top -- LOCOS -- it is the sectional view which it is the sectional view which performed isolation, and (b) formed the polish recon film in the whole surface by law, and carried out the ion implantation of the n mold impurity to the surface, and (c) is the sectional view which formed the silicon oxide film on the polish recon film further.
[Drawing 4] Drawing 4 is drawing showing the outline of each process of manufacture of the semiconductor device of the 2nd operation gestalt of this invention. (d) is a sectional view in the middle of being the sectional view on which the silicon oxide film was processed, and (e) having carried out dry etching of the part which the impurity of the polish recon film surface section contains from the condition shown in (d) from the condition shown in drawing 3 (c), and (f) is the sectional view which carried out dry etching of the part which does not contain the impurity of the polish recon film, and formed the gate electrode from the condition shown in (e).
[Drawing 5] Drawing 5 is drawing showing the outline of each process of manufacture of the semiconductor device of the 2nd operation gestalt of this invention. From the condition shown in drawing 4 (f), (g) removes the silicon oxide film which exists between the gate electrode edge section and a component demarcation membrane, and carries out the ion implantation of the n mold impurity there. n - It is the sectional view in which the field was formed. (h) From the condition shown in (g), after forming a sidewall, the ion implantation of the n mold impurity is carried out between the sidewall edge section and a component demarcation membrane, and it is n+. It is drawing in which the field was formed. (i) It is the sectional view which removed the silicon oxide film on a gate electrode from the condition shown in (h) by etching.
[Drawing 6] Drawing 6 is drawing showing the outline of each process of manufacture of the semiconductor device of the 2nd operation gestalt of this invention. (j) is the sectional view which

formed the titanium silicide film on silicon from the condition shown in drawing 5 (i), and (k) is drawing in which the condition shown in (j) to the interlayer insulation film was formed on the whole surface.

[Drawing 7] Drawing 7 is drawing showing each process of the formation approach of the gate electrode by the conventional dry etching method. (a) forms the polish recon film through an insulator layer on a semi-conductor substrate. After carrying out the ion implantation of the impurity to the surface section, it is the sectional view which formed the silicon oxide film and performed predetermined processing by predetermined etching. (b) Then, it is the sectional view which carried out dry etching of the polish recon film, and formed the gate electrode, and (c) is the sectional view in which the sidewall was formed, after removing the insulator layer of a gate electrode periphery.

[Drawing 8] Drawing 8 is drawing showing each process of the formation approach of the gate electrode by the conventional dry etching method. (d) is the sectional view which removed the silicon oxide film on a gate electrode from the condition shown in drawing 7 (c) by etching, and (e) is the sectional view which formed the titanium silicide film on silicon from the condition shown in (d).

[Description of Notations]

1 16 [-- An impurity, 5, 10 20 / -- The silicon oxide film, 6 / -- A p-type silicon semi-conductor substrate, 7 / -- A component demarcation membrane, 9 / -- 11 n mold impurity, 21 / -- Gate oxide, 12 / -- n-field, 13 / -- n+ / 14 A field, 22 / -- Interlayer insulation film / -- 15 A sidewall, 23 -- Titanium silicide, 16] -- 2 A semi-conductor substrate, 17 -- An insulator layer, 3, 8, 18 -- 4 A polish recon layer, 19

[Translation done.]

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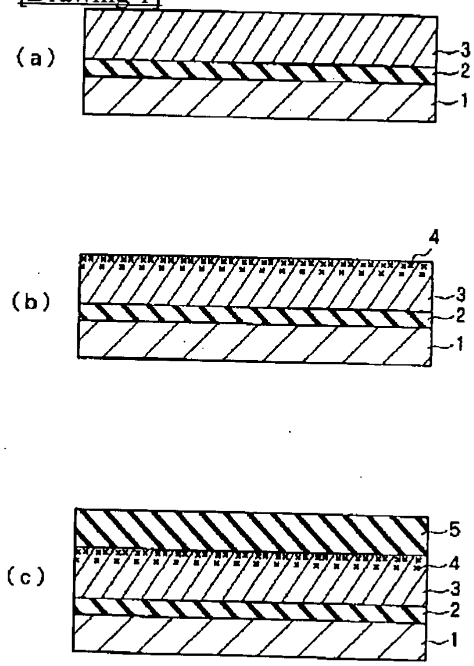
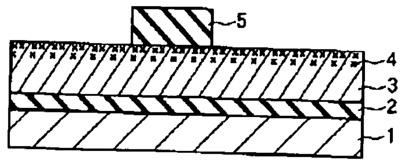
DRAWINGS

[Drawing 1]

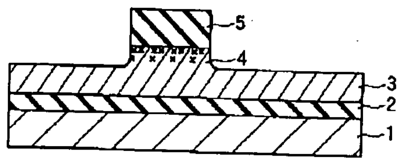


[Drawing 2]

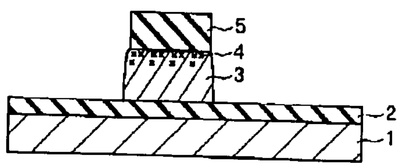
(d)



(e)

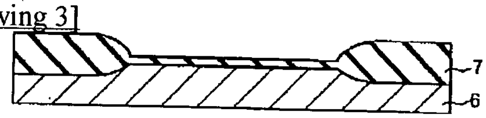


(f)

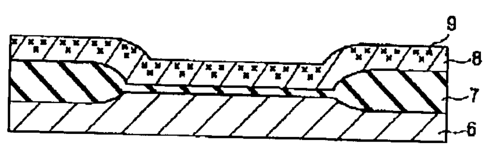


[Drawing 3]

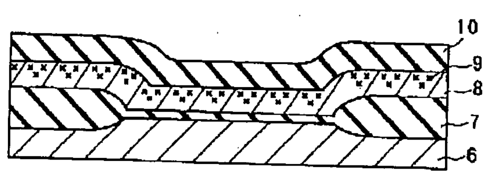
(a)



(b)

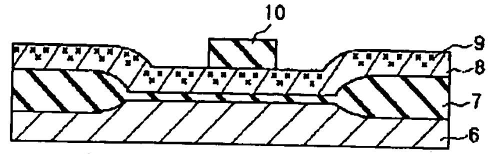


(c)



[Drawing 4]

(d)



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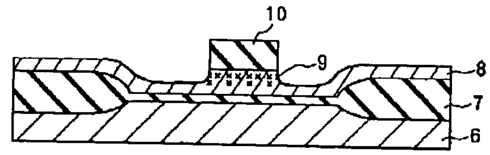
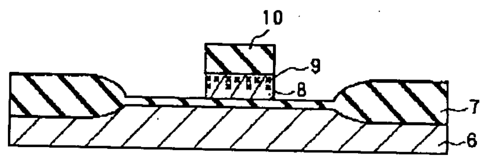
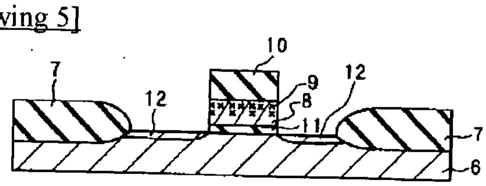


(f)

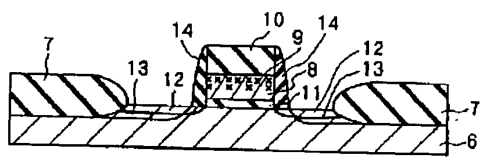


[Drawing 5]

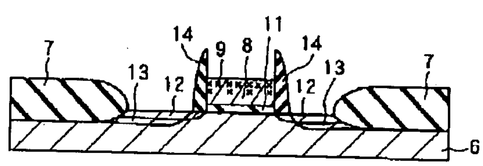
(g)



(h)



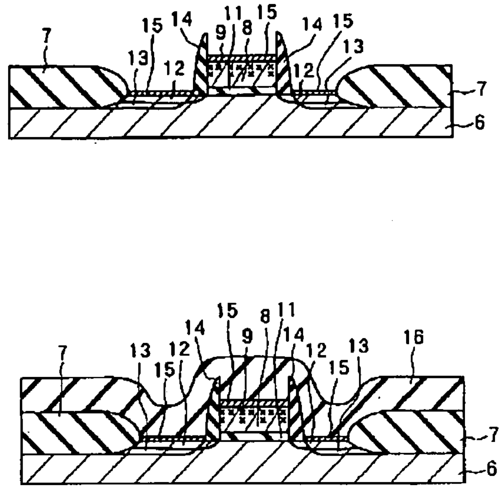
(i)



[Drawing 6]

(j)

(k)

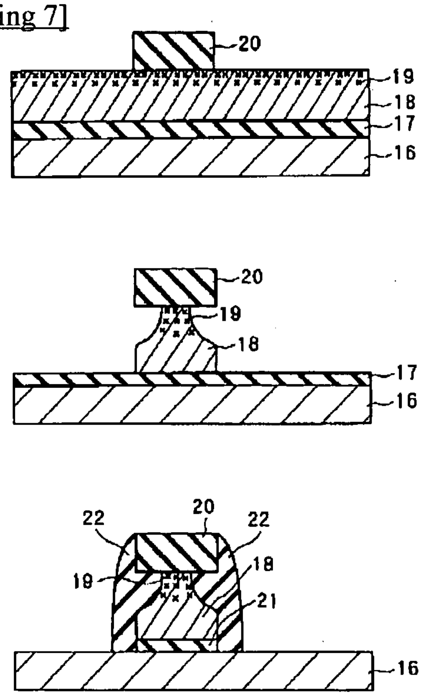


[Drawing 7]

(a)

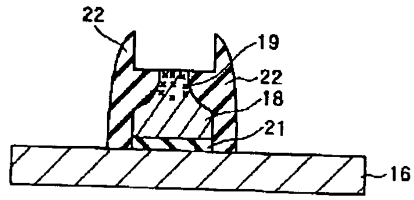
(b)

(c)

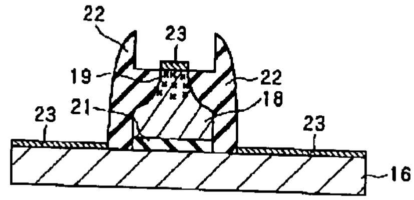


[Drawing 8]

(d)



(e)



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